REMARKS

In response to the Office Action mailed on 29th July, 2004, Applicant presents for entry the following remarks for the Examiner's consideration. Claims 1, 12, 14, 19, 21, and 26-31 are pending in the application. Upon entry of this amendment, the status of the claims will be as set forth in the above listing of the claims.

Rejection of claims under 35 USC §103

Claims 1-3, 12, 14, 19, 21 and 26-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Menon et al. in view of Aude et al.

The base reasoning relied upon by the Examiner in the rejection of the independent claims 1, 12 and 19 is that while Menon et al. discloses all other elements of these claims, it does not disclose the differential logic circuit fabricated of thin oxide transistors and the current source fabricated using at least one thick oxide transistor by a fabrication process, but the Aude et al. reference does. Applicant agrees that Menon et al. fails to teach these recitations of the claims 1, 12 and 19, and dependents therefrom, but must respectfully disagree that the Aude et al. reference cures this shortcoming.

Independent claims 1, 12, and 19 each recite that the thin and thick oxide transistors are fabricated using *a fabrication process* (singular) capable of creating both thick and thin oxide transistors. The specification describes this process in numerous places, including at page 5, lines 2-21; page 6, lines 8-13; and page 8,

lines 1-13. Page 5, lines 3-5, for instance, states, "The present invention is applicable to CMOS circuits fabricated using a process wherein two types of CMOS transistors can be fabricated." This passage then goes on to describe the meaning of thick and thin oxide transistors as a function of the relationship of the thickness of oxide layers with respect to one another. Page 6, lines 8-13, states, "Thus, for purposes of this document, the exact dimensions and other parameters are unimportant and the terms "thin" and "thick" in this context are intended to be by this definition relative terms for devices fabricated using a semiconductor manufacturing process capable of fabricating **both** relatively thick and relatively thin oxide transistors, when viewed in comparison with one another." (emphasis added) This passage makes it clear that the process is a process capable of fabricating both thin and thick oxide transistors. Similarly, page 8, lines 1-13, states in relevant part, "As previously discussed, the present invention is realized by way of a fabrication process which provides for the ability to fabricate CMOS transistor devices as ***either*** thick oxide transistor devices (capable of relatively high voltage, but comparatively slow) or thin oxide transistor devices (with relatively high switching speed, relatively high transconductance g_m, but relatively low maximum voltage swing). In this case, the current source is fabricated using one or more thick oxide transistor devices such as transistor 44. Logic device 30 (as a representative of many such logic devices) is fabricated using thin oxide transistors such as 48 and 52. The bias load circuit, as represented by transistors 56 and 60 connected from the sources of transistors 48 and 52 respectively to ground, ***may be fabricated as either*** thick oxide or thin oxide transistors, or may even be a passive device such as a resistor without departing

from the invention." (emphasis added) Applicant respectfully submits that these passages make it clear that the fabrication process, by being able to fabricate either thick or thin devices, is of course capable of fabricating both types of thicknesses of oxide transistors.

Such is not the case with the Aude et al. reference. The Aude et al. reference explicitly and repeatedly states and, indeed requires, that two separate processes be used to fabricate transistors of varying thickness. Column 2, lines 53, 61; column 3, lines 14-22; page 5, line 62 to column 6, line 7; and column 6, lines 33-45 all state that the thick oxide FETs are fabricated "using a first process" and that the thin-oxide FET is "fabricated using a second process..." The Examiner is additionally referred to the Abstract and the Claims of the Aude et al. reference. There is no teaching or suggestion by Aude that these two processes are part of the same process.

There additionally is no teaching, suggestion or other disclosure within the Aude et al. reference that countermands these strong statements in the reference. In fact, a process capable of fabricating both thin and thick oxide transistors (per the present claimed invention) is against the teachings of the Aude et al. reference.

The independent claims 1, 12, and 19 have been amended to include recitations that were persuasive in the allowance of claims in the parent application, now U.S. Patent No. 6,731,136, thus bringing the recitations of the currently pending method claims more in harmony with the allowed structure claims of the '136 patent.

Claims 2 and 3 have been canceled as the subject matter of these claims is now in claim 1. Claims 14, 21, and 26-31 depend from the base claims. These claims are thus believed to be patentably distinct as well.

In view of this communication, a Notice of Allowability of all the pending claims is eagerly awaited at the Examiner's first convenience. The undersigned may be contacted if there are any questions about this filing.

Respectfully submitted,

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